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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/088,674	06/02/1998	DANIEL J. MORGAN	TI-25995	2025

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EXAMINER	
NGUYEN, KEVIN M	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/088,674	MORGAN ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 11/15/2004, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3 and 5-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al (previously cited, US 6,222,515).

3. As to claim 1(currently revised), Yamaguchi et al teach a system of displaying digital video data associated with a method comprising: a first pixel value defined by [(3V) is mean effective voltage], see fig. 7B.

Yamaguchi et al further teach inherently a first predetermined amount "-1" [defined by an area hatching from 3V to 2V at the first field] to form a first offset pixel value [defined by 2V at the first field], and a displaying said first offset pixel during a first frame period [2V at the first filed, see fig. 7B];

Yamaguchi et al further teach inherently the opposite of said predetermined amount "+1" [defined by an area hatching from 3V to 4V at the first field] to form a second offset pixel value [defined by 4V at a second field], and a displaying said second offset pixel during a second frame period [4V at the second filed, see fig. 7B];

Yamaguchi et al further teach the average of said displayed first offset pixel value [2V at the first filed] and said second offset pixel value [4V at the first filed] is said first pixel value (3V) [(3V) is mean effective voltage which is shown by area hatching in figure 7B" (see fig. 7B, col. 8, lines 11-27)].

4. As to claim 6 (currently revised), Yamaguchi et al teach inherently a logic circuit defined by means for offsetting inherently a first predetermined amount "-1" [defined by an area hatching from 3V to 2V at the first field] to form a first offset pixel value [defined by 2V at the first field]

Yamaguchi et al further teach inherently a logic circuit defined by means for offsetting inherently by the opposite of said predetermined amount "+1" [defined by an

area hatching from 3V to 4V at the second field] to form a second offset pixel value [defined by 4V at a second field].

Yamaguchi et al further teach a display panel 19 (display means, fig. 1B) which displays said first offset pixel during a first frame period [2V at the first filed, see fig. 7B], and displays said second offset pixel during a second frame period [4V at the second filed, see fig. 7B].

Yamaguchi et al further teach the average of said displayed first offset pixel value [2V at the first filed] and said second offset pixel value [4V at the first filed] is said first pixel value (3V) [(3V) is mean effective voltage which is shown by hatching in figure 7B" (see fig. 7B, col. 8, lines 11-27).

5. As to claims 2 and 7 (currently revised), Yamaguchi et al teach inherently said first predetermined amount "-1" [defined by 2V-3V at the first field], said predetermined amount "+1" [defined by 4V-3V at the first field]. Thus, said first predetermined amount "-1" is selectively as a function of (X-3).

6. As to claims 3 and 8, Yamaguchi et al teach said first offset pixel value 2V is less than said first pixel value (3V) as a function (X-3) of the spatial location ["-1" defined the spatial location] that [(3V) is mean effective voltage] defined to be displayed.

7. As to claims 5 and 10 (currently revised), Yamaguchi et al show the fig. 7 including the first field are consecutive the second field.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al in view of Aras et al (newly cited, US 5,731,802).

9. As to claims 4 and 9 (currently revised), Yamaguchi et al teach all of the claimed limitations of claims 1 and 6, except for display uses a plurality of weighted bit-plane, wherein said first pixel values close to a bit transition of said bit-planes are offset during said display frame and said second frame.

However, Aras et al teach the number of rows multiplied by the number of bits in grayscale weighting is equal to the number of update event per frame or write cycle per frame (fig. 4, col. 5, lines 32-34). Rows 0, 1 and 2 are loaded with the data for the 0^{th}, 3^{rd} and 2^{nd} weight bits, respectively. The number of data transitions per clock cycle during the next clock cycle of the data in rows 1 and 2 changes such that rows 1 and 2 are loaded with the data for its 0^{th} and 3^{rd} weight bits, respectively (col. 6, lines 26-37).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Yamaguchi et al's field (frame, fig. 7) including rows 0, 1 and 2 are loaded with the data for the 0^{th}, 3^{rd} and 2^{nd} weight bits, respectively. The number of data transitions per clock cycle during the next clock cycle of the data in rows 1 and 2 changes such that rows 1 and 2 are loaded with the data for its 0^{th} and 3^{rd} weight bits, respectively, in view of the teaching in the Aras et al's reference, because this would provide gray scale using a weighted PWM scheme which does not flicker and

provides a reduced bandwidth requirement for the associated control circuitry and data bus as taught by Aras et al (col. 3, lines 41-44).

Response to Arguments

10. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Nguyen whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KMN
February 1st, 2005

PATRICK N. EDOUARD
PRIMARY EXAMINER